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FIG.1

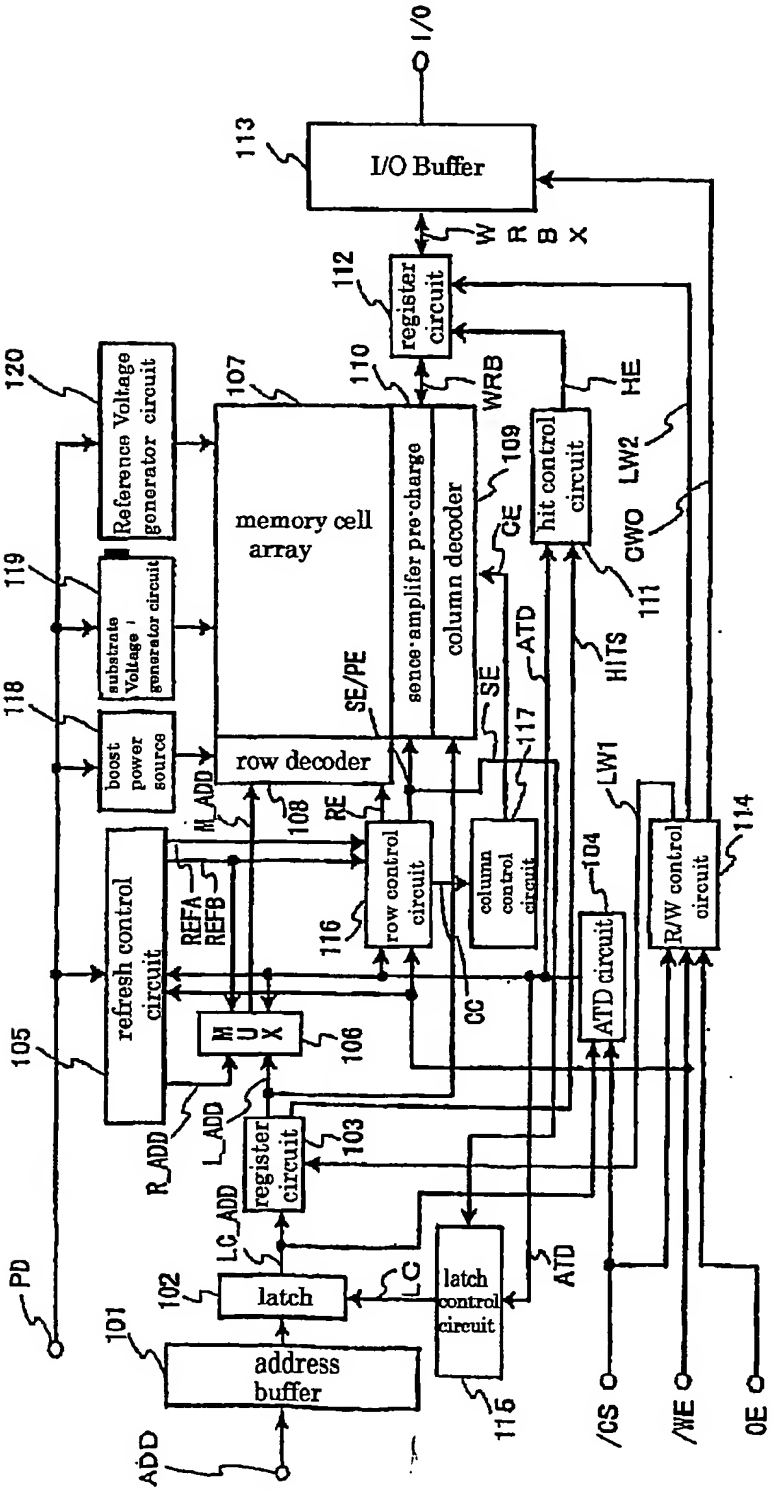

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FIG.2

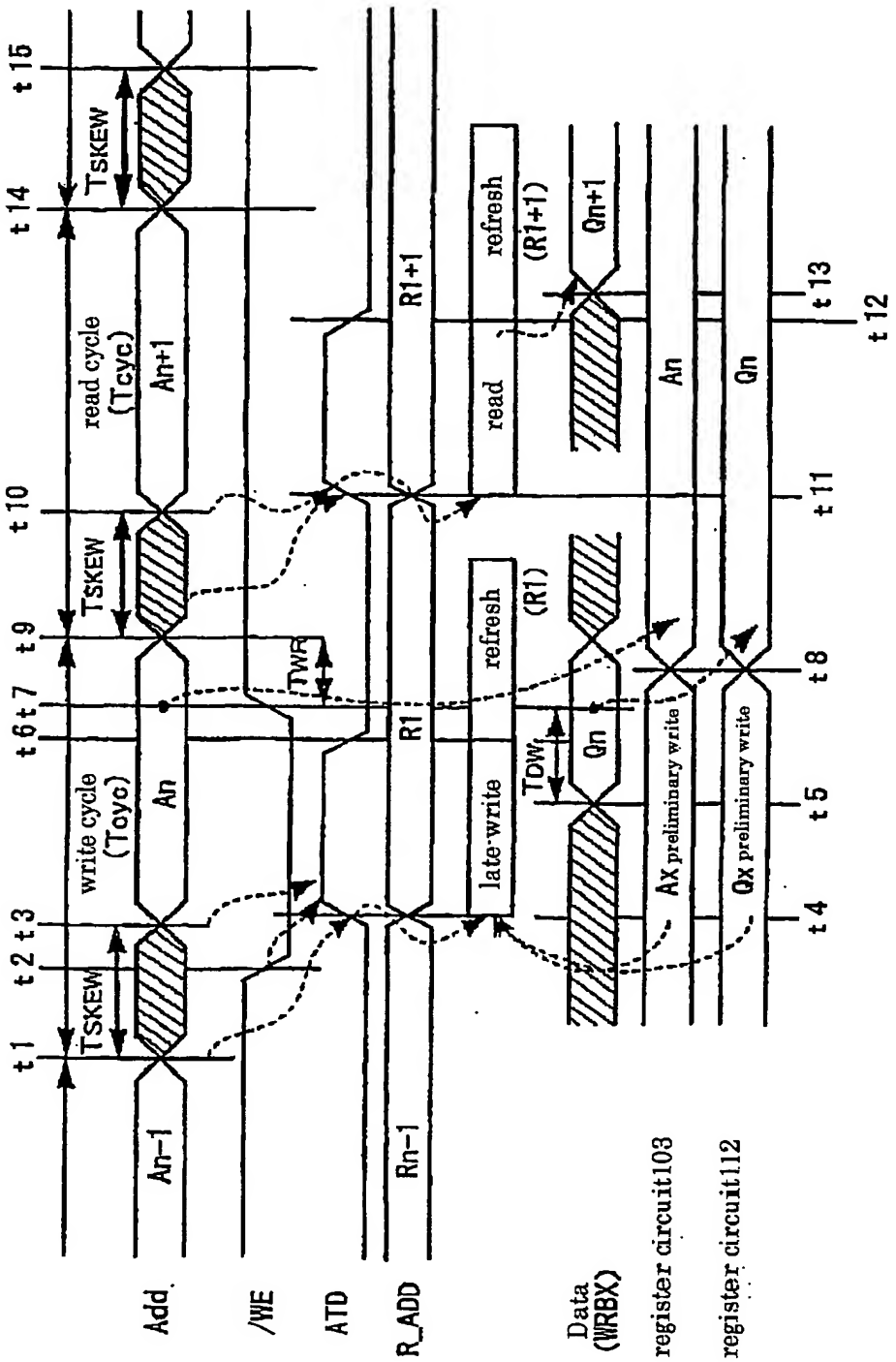

FIG.3

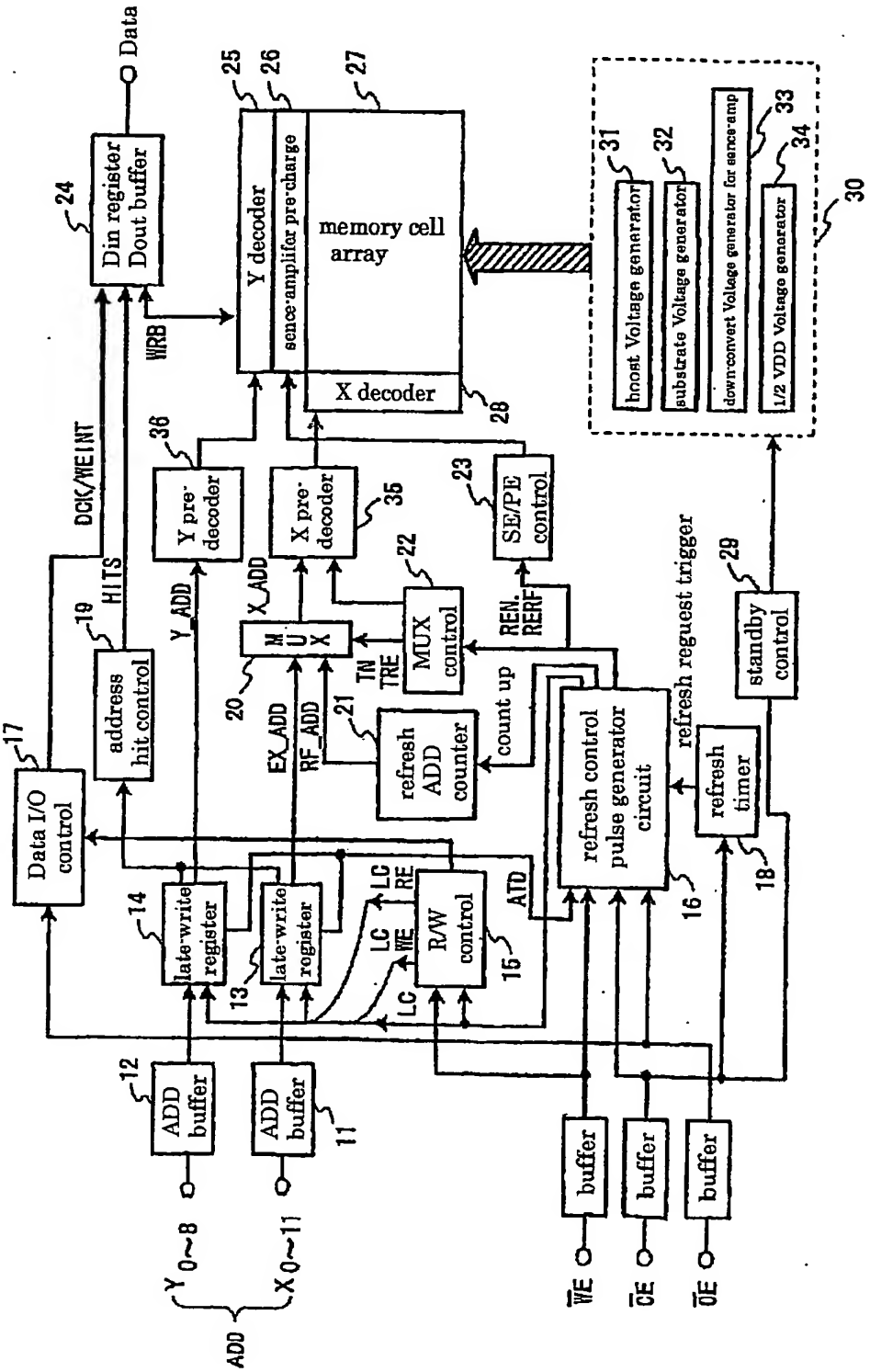
Data
Din register Dout buffer
24
25
Y decoder
26
sence-amplifer pre-charge
27
memory cell array
X decoder
28
30
boost Voltage generator
31
substrate Voltage generator
32
down-convert Voltage generator for sence-amp
33
1/2 VDD Voltage generator
34
WRB
DCK/WEINT
HITS
Y_ADD
X_ADD
Y pre-decoder
36
X pre-decoder
35
SE/PE control
23
MUX control
22
REN. RERF
standby control
29
refresh request trigger
address hit control
19
MUX
20
TN TRE
EX_ADD
RF_ADD
21
refresh ADD counter
count up
refresh control pulse generator circuit
16
refresh timer
18
Data I/O control
17
late-write register
14
late-write register
13
LC WE
LC RE
LC
R/W control
15
ATD
ADD buffer
12
ADD buffer
11
buffer
buffer
buffer
Y 0~8
X 0~11
ADD
WE
CE
OE

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FIG.4

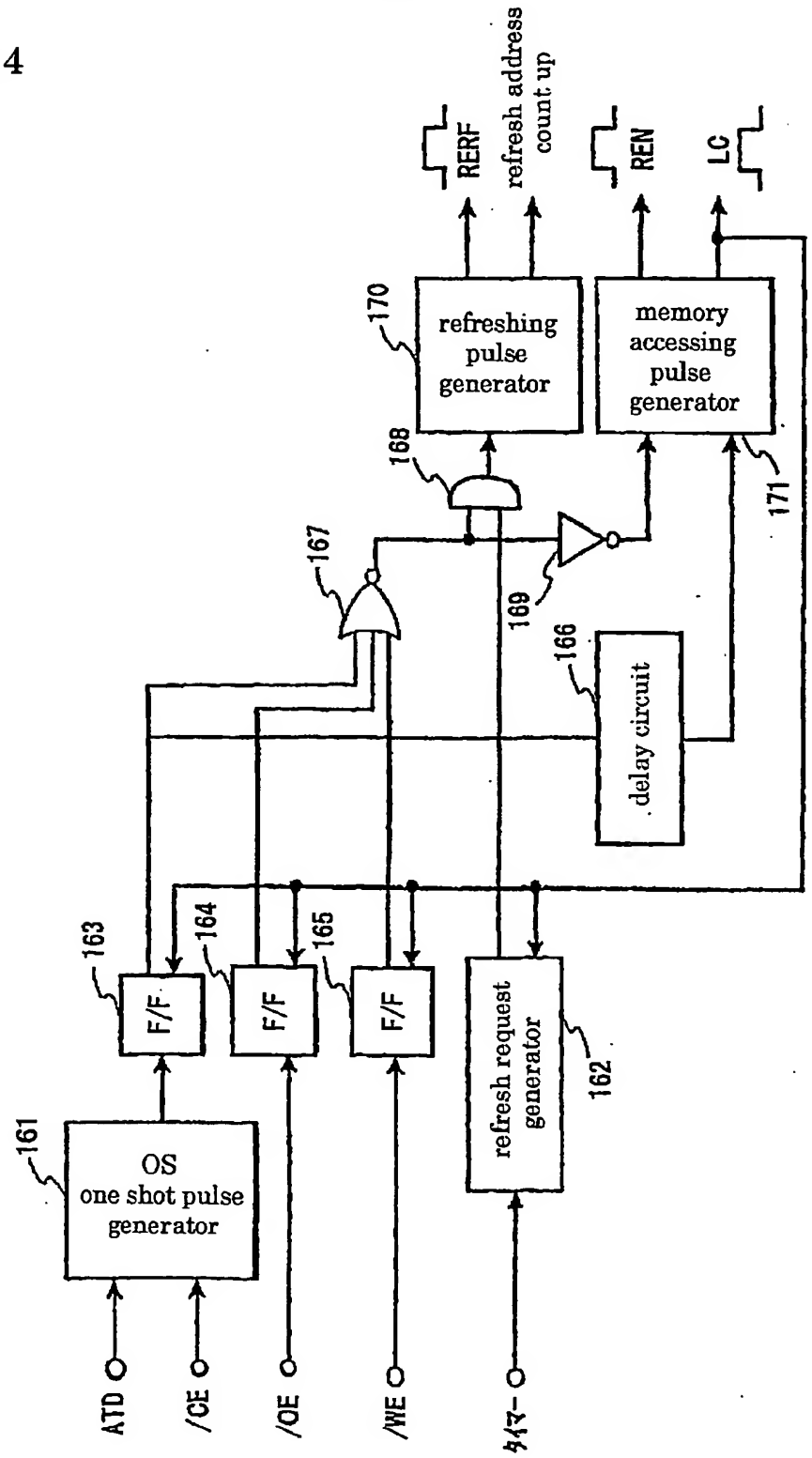

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FIG.5

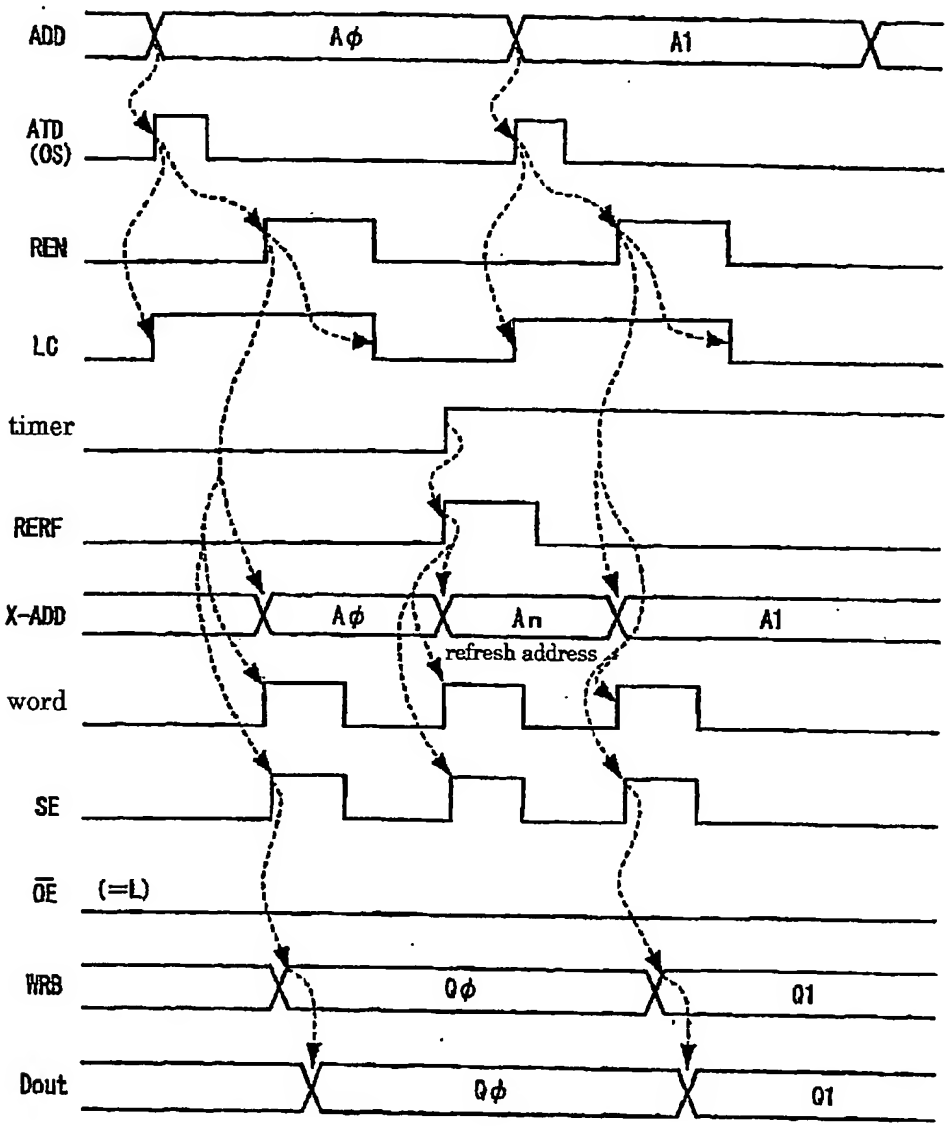

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FIG.6

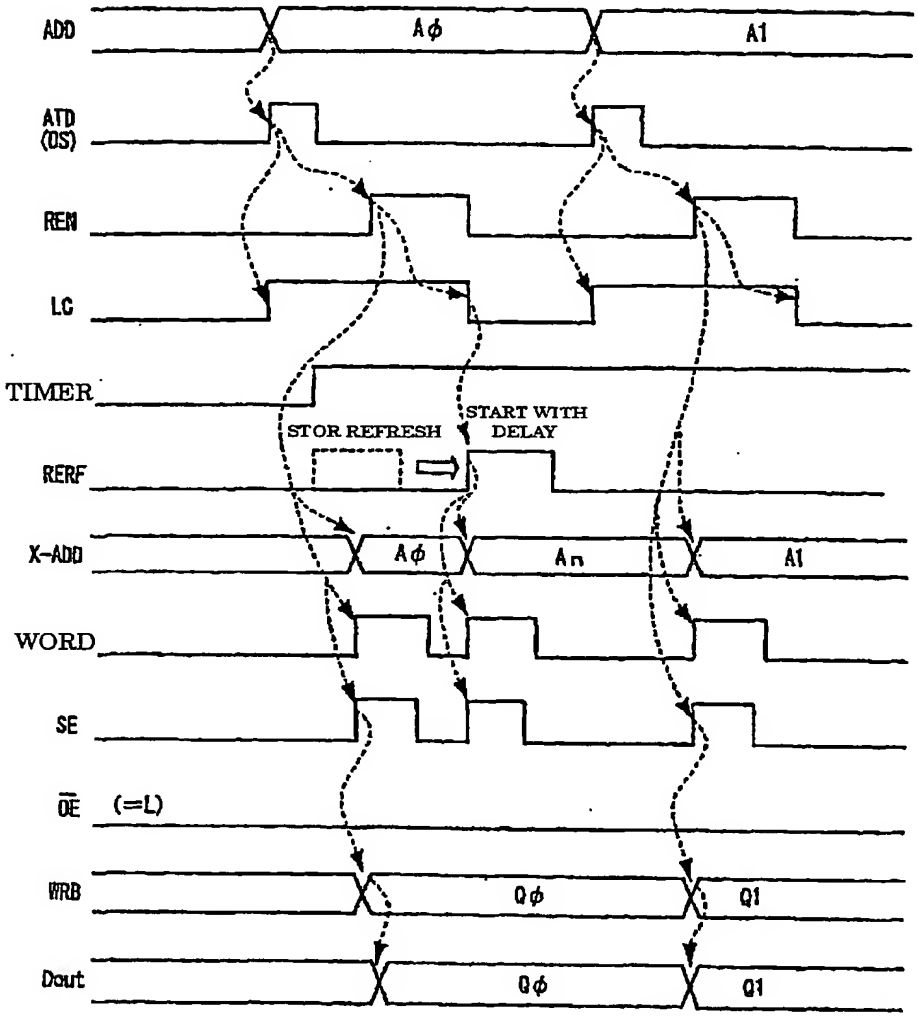

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FIG.7

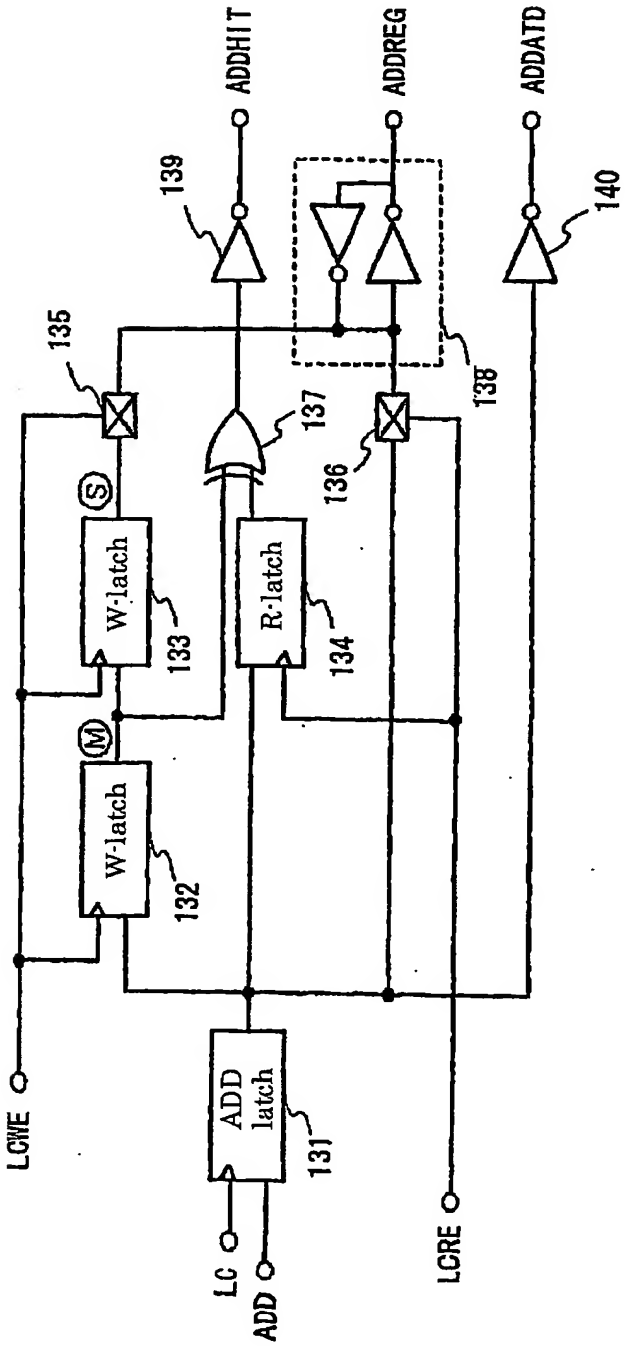

FIG.8

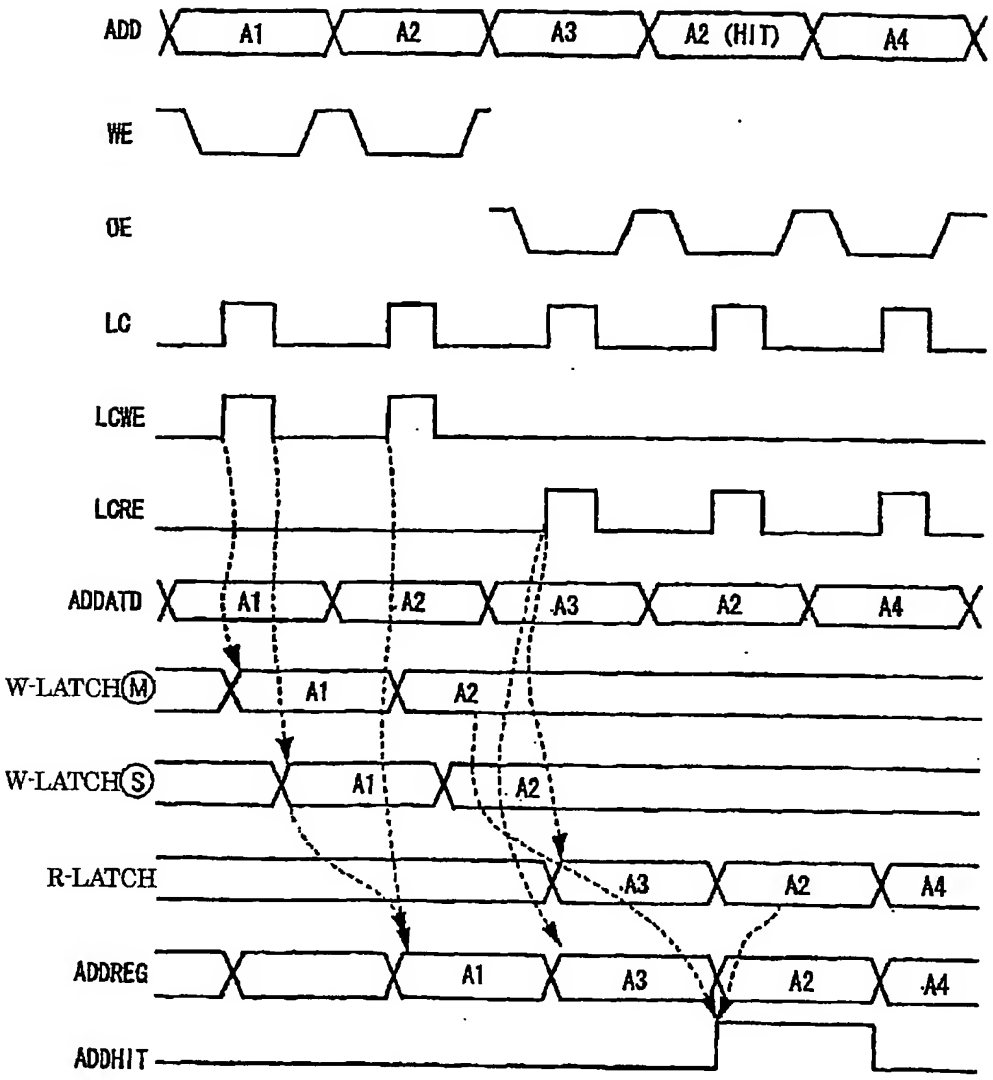
ADD
A1
A2
A3
A2 (HIT)
A4
WE
OE
LC
LCWE
LCRE
ADDATD
A1
A2
A3
A2
A4
W-LATCH(M)
A1
A2
W-LATCH(S)
A1
A2
R-LATCH
A3
A2
A4
ADDREG
A1
A3
A2
A4
ADDHIT

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FIG.9

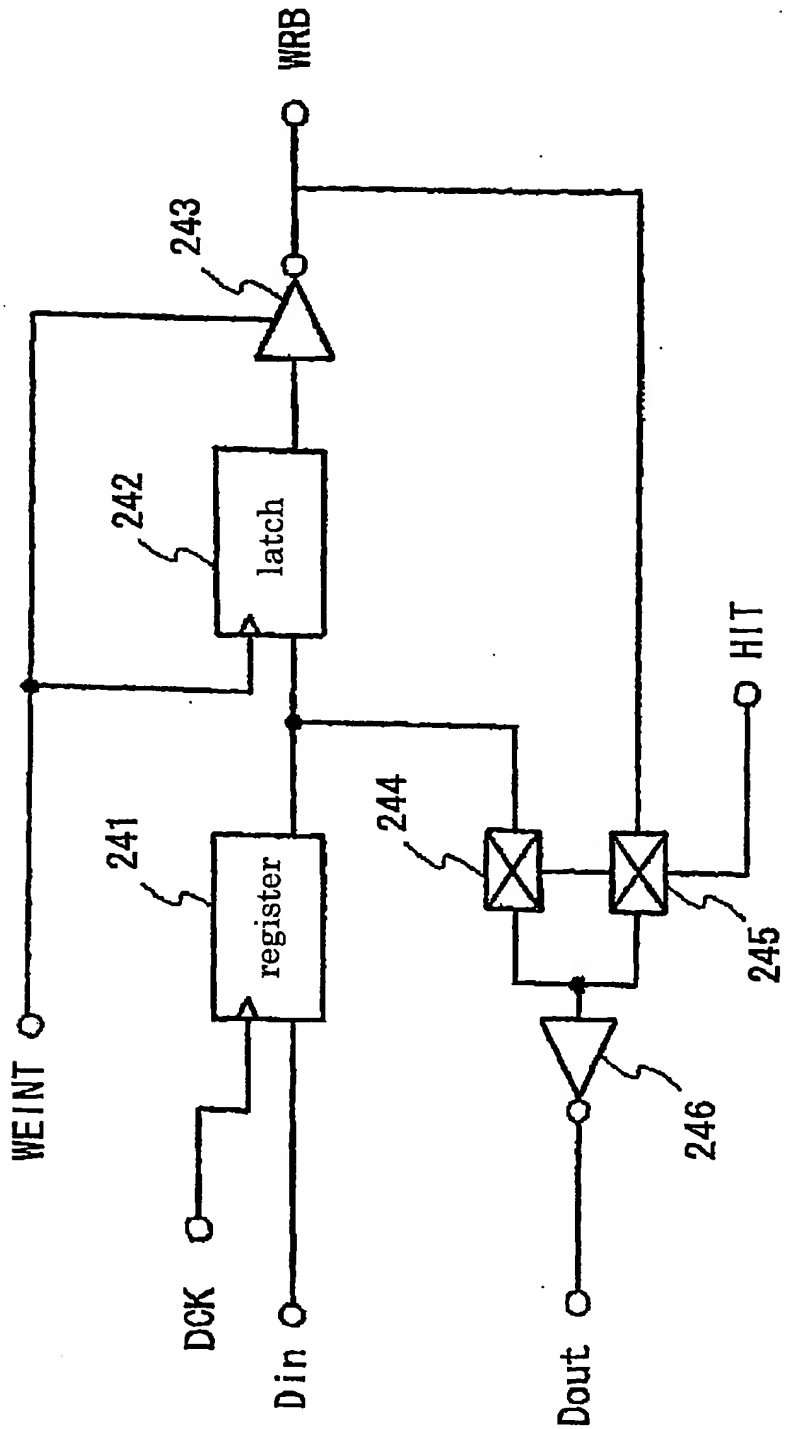

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FIG.10

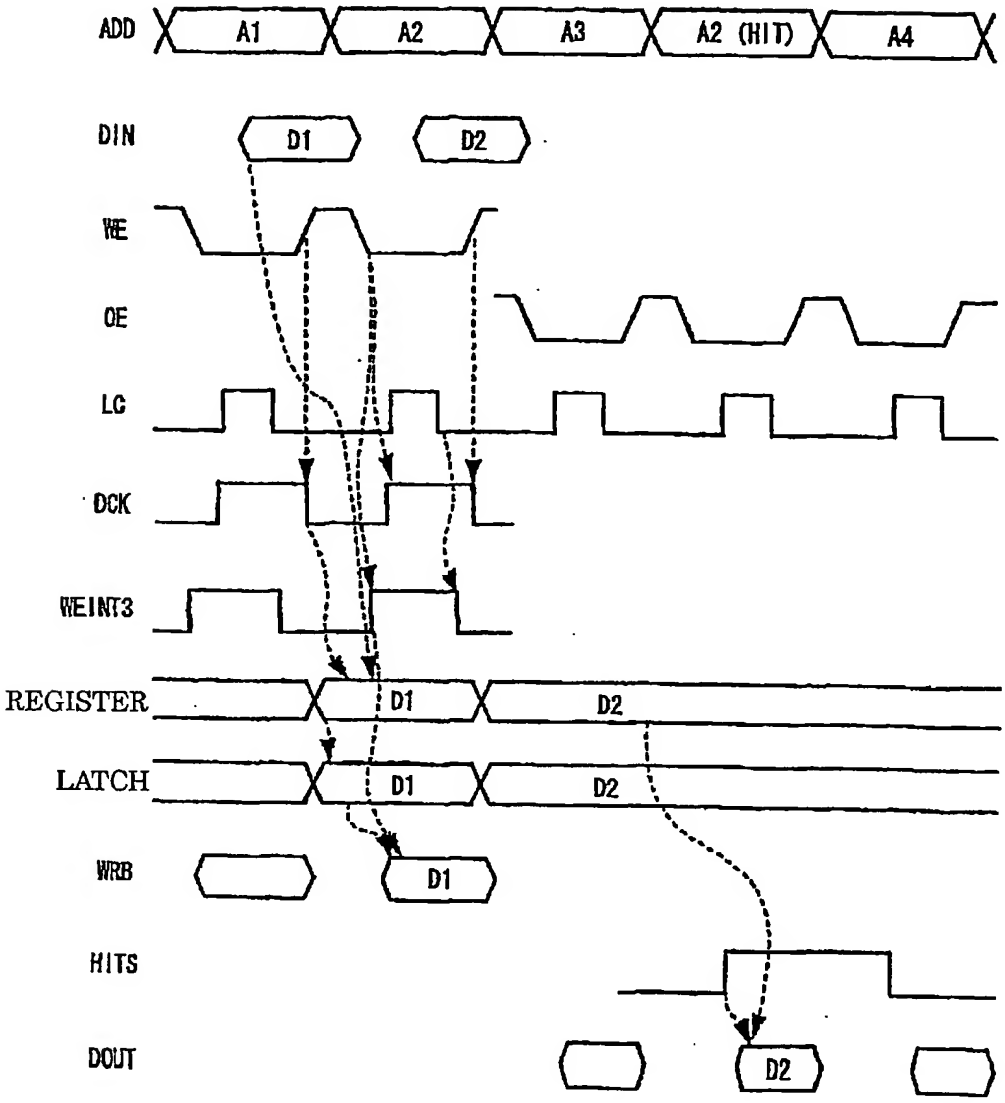

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FIG.11

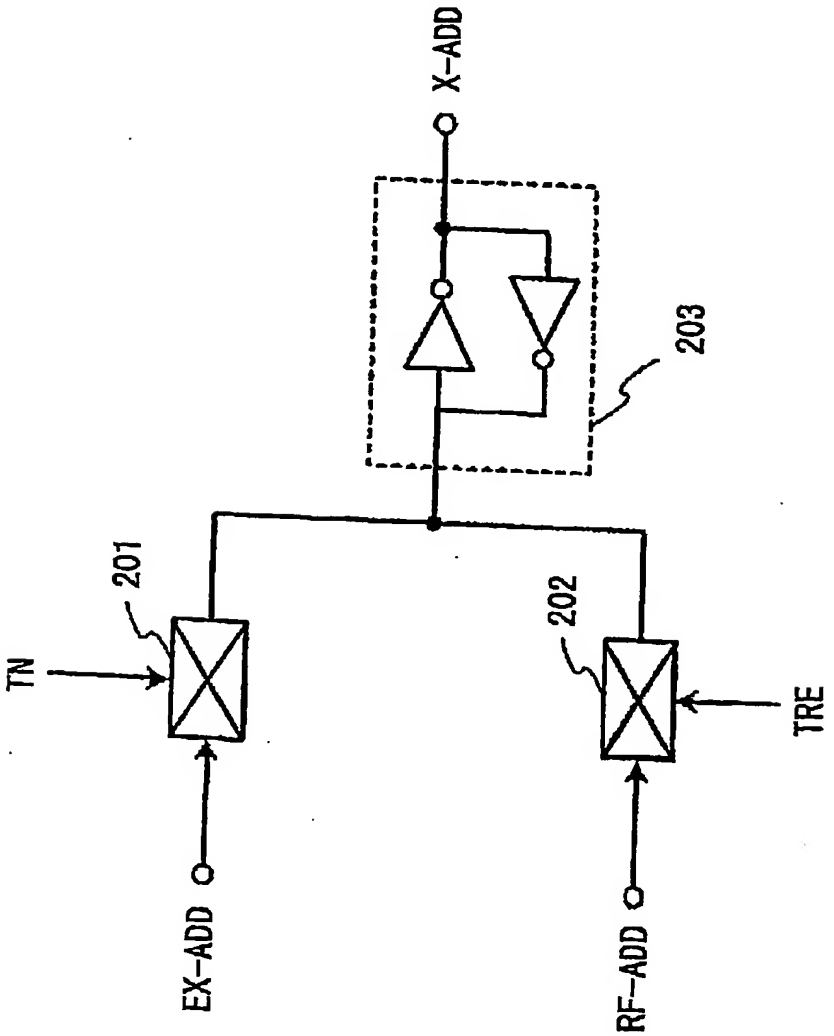

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FIG.12

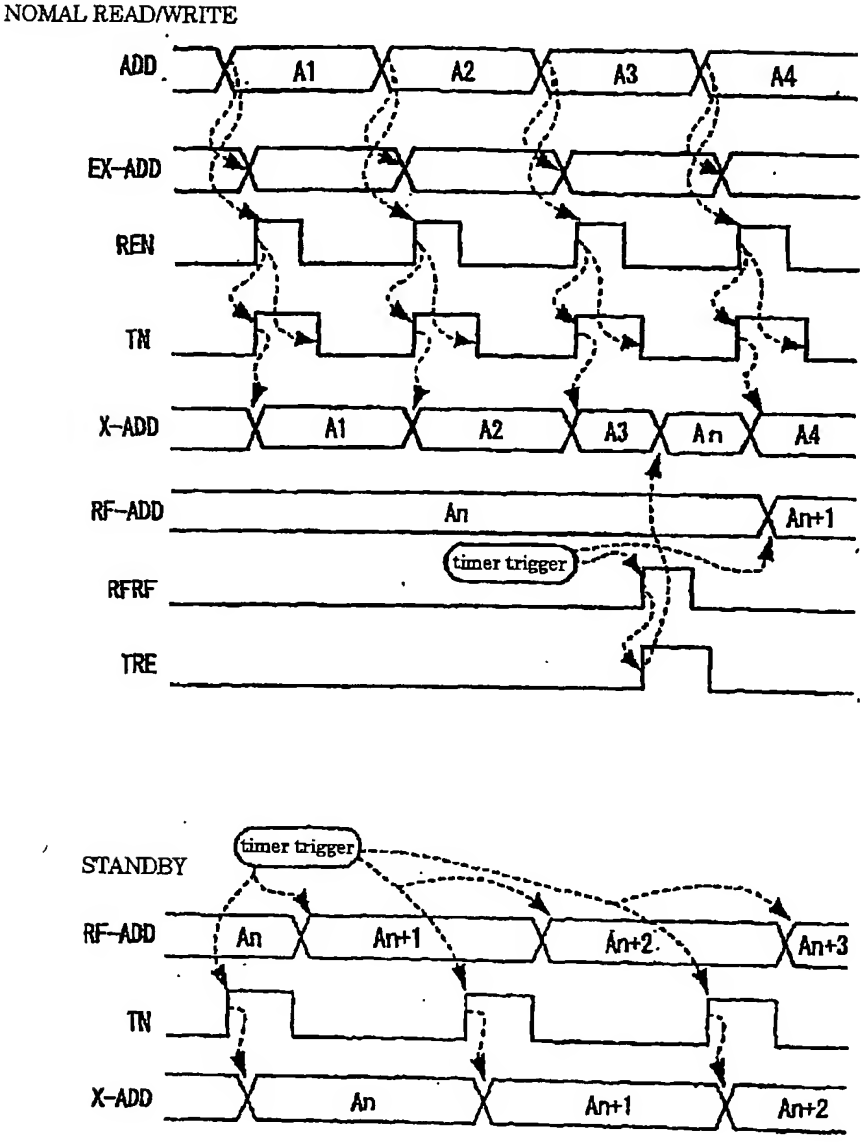

FIG.13

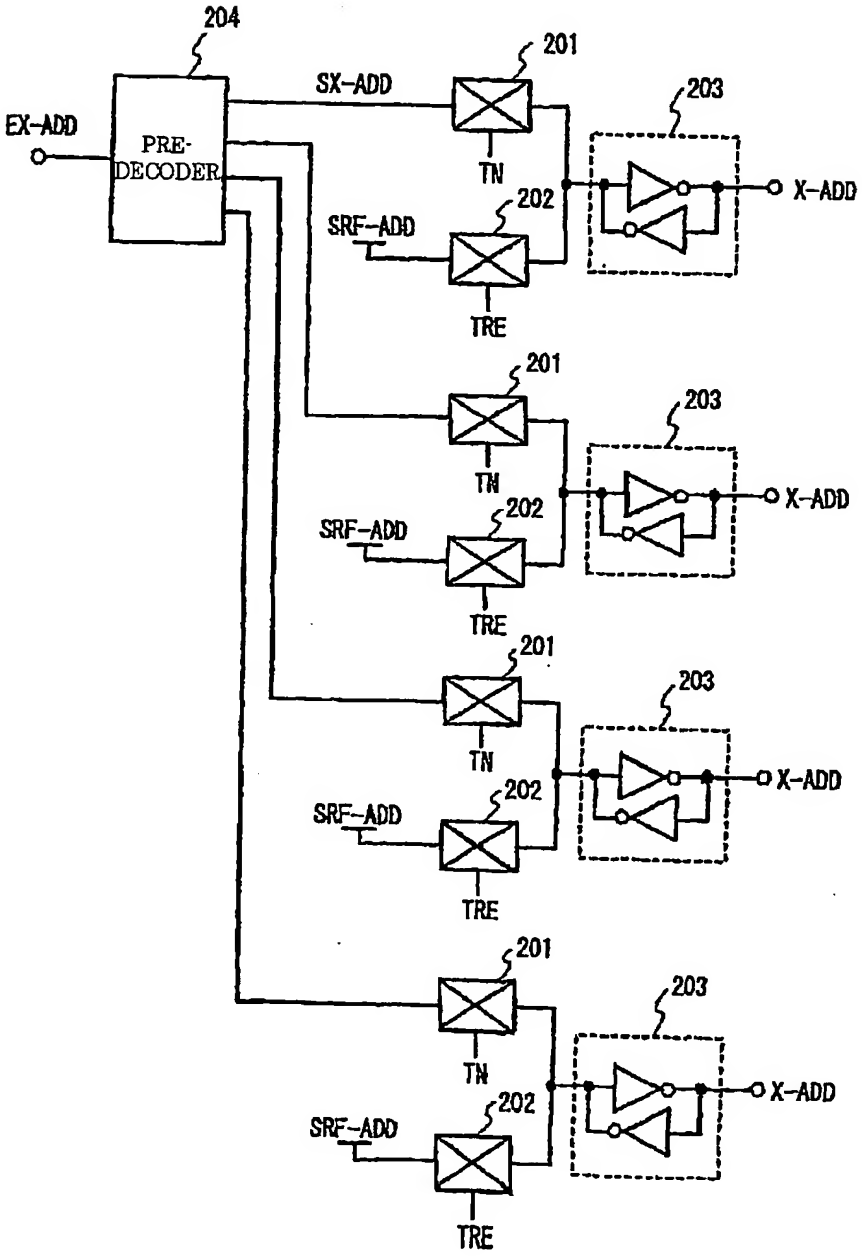

FIG.14

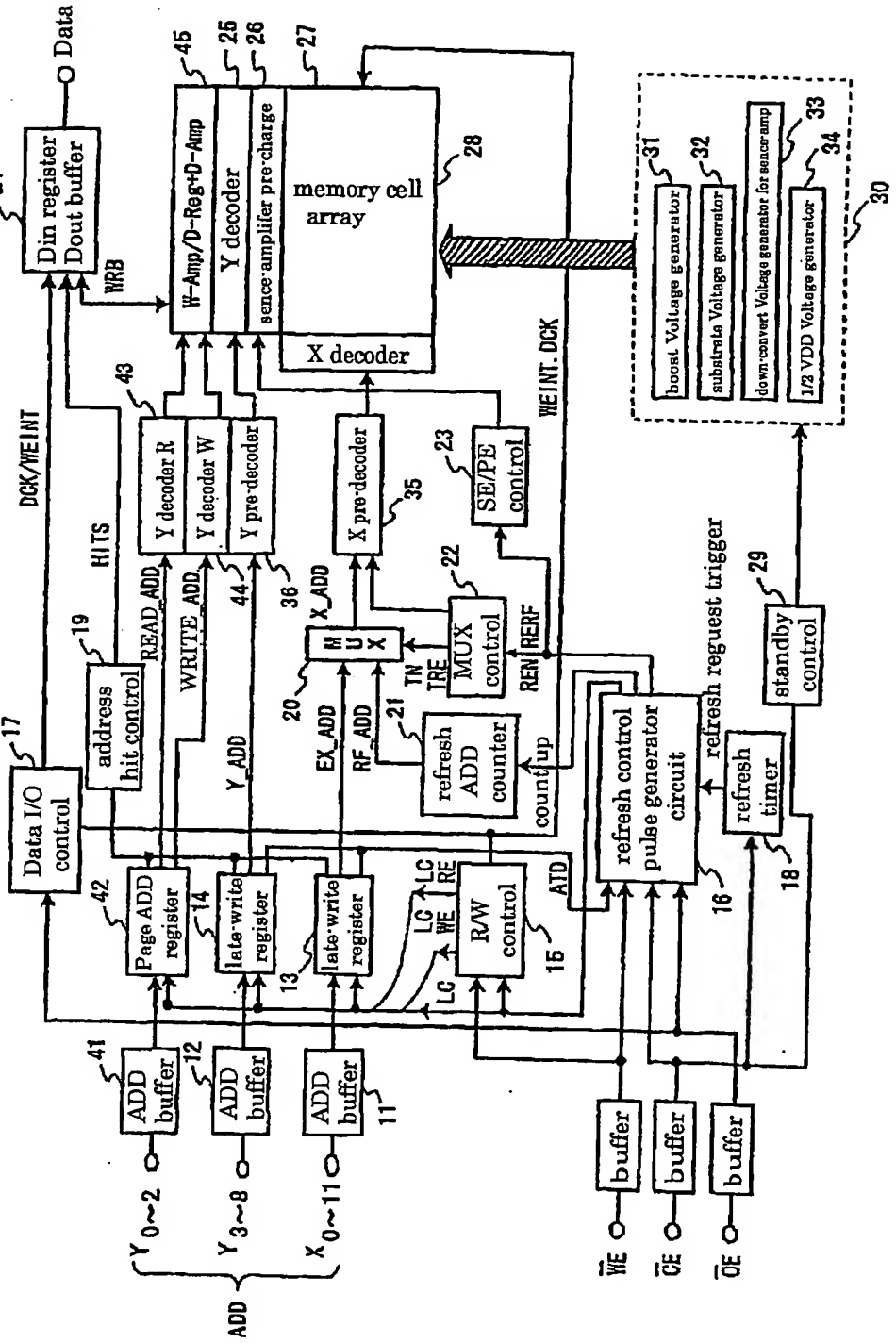
Data
Din register
Dout buffer
WRB
W-Amp/D-Reg+D-Amp
Y decoder
sence-amplifer pre-charge
memory cell array
X decoder
boost Voltage generator
substrate Voltage generator
down-convert Voltage generator for sence-amp
1/2 VDD Voltage generator
WEINT. DCK
DCK/WEINT
HITS
Y decoder R
Y decoder W
Y pre-decoder
X pre-decoder
SE/PE control
READ_ADD
WRITE_ADD
Y_ADD
X_ADD
EX_ADD
RF_ADD
MUX
MUX control
TN
IRE
REN
RERF
address hit control
refresh ADD counter
count up
refresh control pulse generator circuit
refresh request trigger
refresh timer
standby control
Data I/O control
Page ADD register
late-write register
late-write register
late-write register
R/W control
LC
WE
RE
ATD
ADD buffer
ADD buffer
ADD buffer
buffer
buffer
buffer
Y0~2
Y3~8
X0~11
ADD
WE
CE
OE

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FIG.15

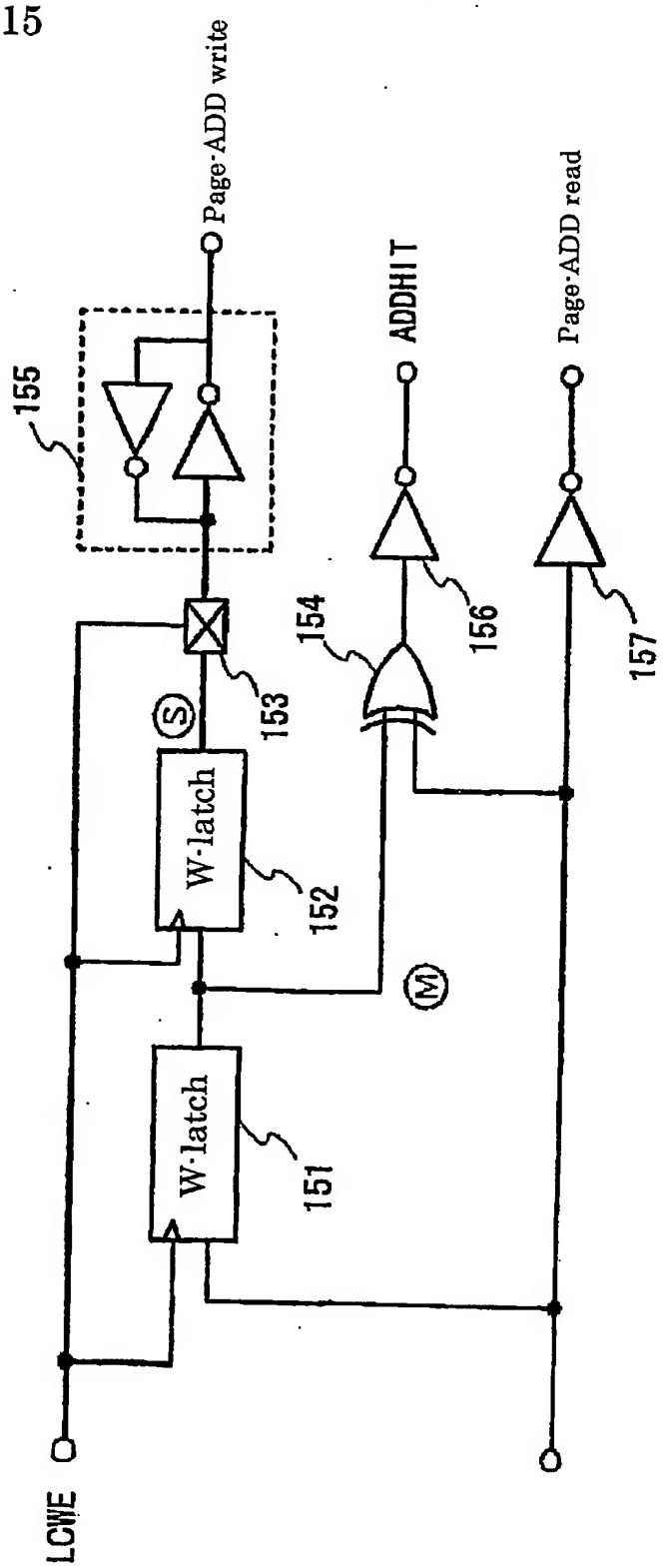

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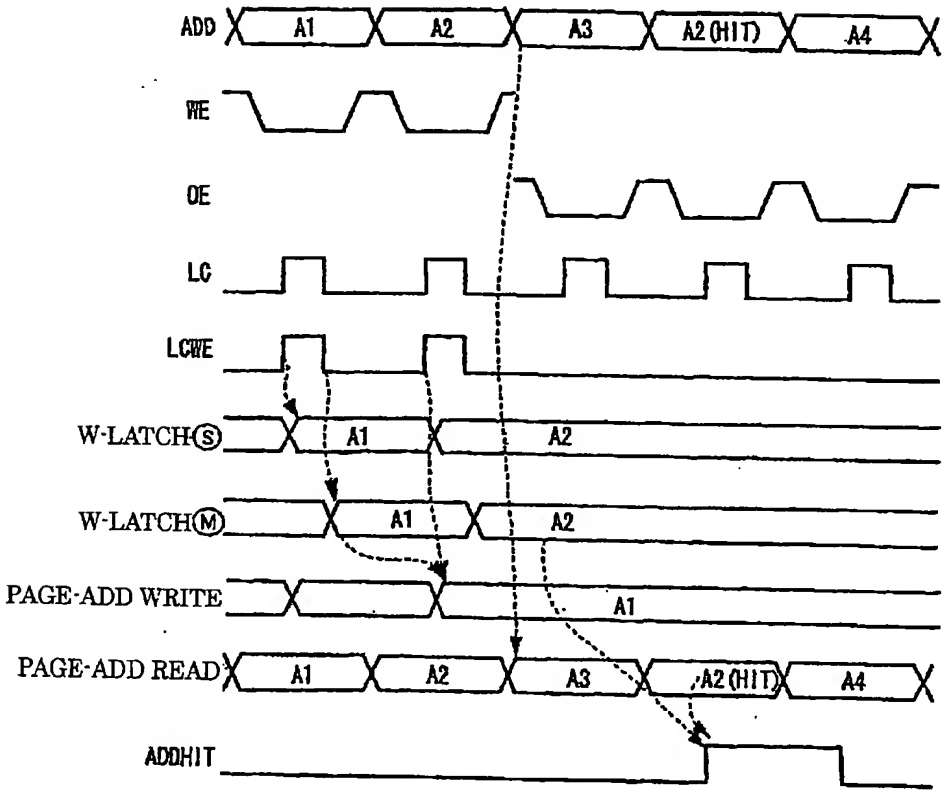
FIG.16



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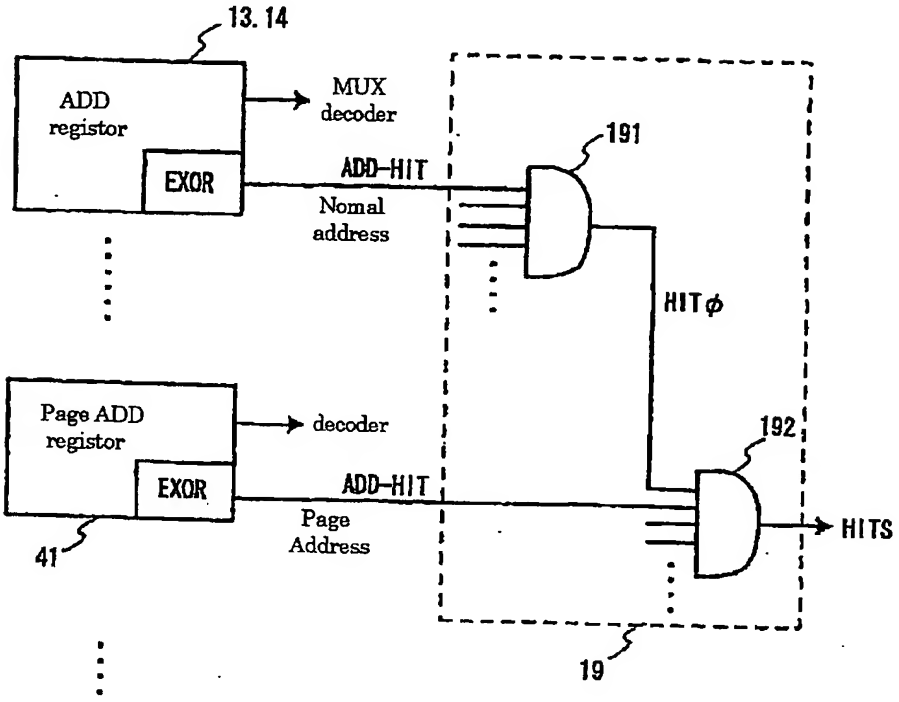
FIG.17